APPLICATION OF TERNARY LOGIC AND DELTA MODULATION
IN DIGITAL FILTER REALIZATION

A. Mavretic, D. Zrilic, R. Zhou
Electrical, Computer and Systems Engineering
Boston University College of Engineering
Boston, MA 02215

ABSTRACT

A new realization of non-recursive digital filters using operation on ternary delta modulated signal is proposed. Direct operation on ternary delta modulated signal will be derived mathematically and a hardware implementation of ternary arithmetic operation will be shown. The primary advantage of the ternary scheme is the simplicity of the hardware and reduction in connections and interconnections between chips and interchips. The results show the possibility of applying ternary arithmetic operation in variety of areas including VLSI environment.

INTRODUCTION

Delta modulation has been discovered for many years. Due to its simplicity in realization and relatively insensitivity to interference, many investigators have been working on developing various delta modulation systems and their applications. Although complete delta modulation systems were developed quite late and relative attention has been given to the application of delta modulation to digital signal processing and communications, digital filter realization based on delta modulation is still very attractive. Several realizations of digital filters using delta modulation have been proposed, they show great advantage over conventional realization of digital filter based on PCM technology\(^{1(2)}\). However, these realizations all use classical binary logic for A/D conversion and its implementation. Binary system, of course, has its advantage but also has its disadvantage when compared with high radix logic system. First, in binary system, one signal line can only carry one bit signal which is either 0 or 1. This will greatly reduce and limit the signal-carrying capability as well as signal processing capability. When we realize a desired logic function in VLSI technology, this will become the limit to the minimum possible size of a chip. We finally will reach the point where further scaling down a signal processing chip is not possible. Second, in VLSI technology the major problems are associated with the complexity of the connections between components on a chip and the interconnections between chips, since information which could be processed by a chip is
proportional to the chip area, but information which could be transferred to the chip by the connecting points is proportional to the chip perimeter. Now the area of a chip increases proportionally to the square of the chip perimeter and the chip perimeter (i.e. the number of pins) becomes the limiting factor in the information processing rather than the chip area. Connection are expensive -- they introduce the usual noise and reliability problems and require expensive testing. As a result, the cost of components is a relatively small part of the total price of the system, while the complexity of interconnections between subsystems dictates the overall cost of the system.

In our case where we use delta modulation technology to realize a digital filter the situation described above becomes more severe: a great number of registers, adders, multipliers, and other devices, rather complicated connections and interconnections, make a VLSI chip design for the filter very difficult, if not impossible. The main issue here is that: Is it possible for one signal line to carry more than one bit information and is it possible for each device to perform more computation? The application of multiple-valued logic and the use of multiple-level delta modulation in digital processing is one way of increasing the information rate per wire \(^{(3)}\), which will lead to a simple inexpensive digital filter implementation where delta modulator acts as a basic A/D convertor and addition and subtraction are carried out in symmetrical non-redundant multiple-valued logic number system.

**TERNARY NUMBER REPRESENTATION AND TERNARY FULL ADDER**

In this paper we consider a symmetrical ternary non-redundant number representation in which the ternary digits are coded as +1, 0, −1. The idea of using ternary logic is not new. The system scientists and engineers who worked on hard problems of synthesis (analysis of a given system is always easier) have asked many times over whether binary logic is optimal. In practice situations frequently arise where binary answer of YES/NO is not sufficient. We would prefer at times a logic systems with statements such as YES/NO/NOT, UP/DOWN/STOP, or RIGHT/LEFT/STRAIGHT-AHEAD. It is obvious that for such realization we would need three valued (radix 3) digital realization. In fact, it has been shown that three is the “best” radix to use, and this also leads to increase of the amount of information per signal line by a factor of 1.585. The symmetric ternary non-redundant number representation is of great interest to digital filter realization. Sign-conversion and special round-off technique are not required, and addition and subtraction carried out without regard to sign \(^{(4)}\). Since the full adder is the base for the subtractor and the multiplier in any radix number system, it is the basic building block in digital signal processing. Thus we first consider the definition of ternary full adder and its mathematical model.
Definition: A ternary full adder is a 3-input and 2-output device which maps input set (3 elements, \(X_n, Y_n, C_{n-1}\)) into output set (2 elements, \(S_n, C_n\)), where all these elements take values of symmetric ternary non-redundant number, i.e. \(X_n, Y_n, C_{n-1}, S_n, C_n \in \{-1, 0, 1\}\). The ternary full adder block diagram is shown in Figure 1. \(X_n, Y_n, C_{n-1}, S_n, C_n\) are named inputs, carry-in, sum and carry-out respectively, as in binary case.

Although input set has \(3^3 = 27\) combinations, only 7 combinations are needed for output set. This is because permutation law applies to addition and we use symmetric non-redundant ternary number system. For addition of three such numbers \((X_n, Y_n, C_{n-1})\), only 7 different outcomes are possible, i.e. if we designate \(Z_n = X_n + Y_n + C_{n-1}\) then \(Z_n \in \{3, 2, 1, 0, -1, -2, -3\}\). Each of these 7 outcomes can be assigned a different pair \((S_n, C_n)\).

There are \(C_7^9 = 36\) possibilities of two ternary delta modulated sequences. They are listed in TABLE 1 and TABLE 2. The two tables can be viewed as the truth tables for ternary full adder.

From TABLE 1 we have

\[
S_n = \frac{1}{3} \left[ X_n + Y_n + C_{n-1} - C_n \right]
\]

From TABLE 2 we have

\[
S_n = \frac{1}{3} \left[ X_n + Y_n + C_{n-1} + C_n \right]
\]

Let us consider \(S_n = \frac{1}{3} \left[ X_n + Y_n + C_{n-1} - C_n \right]\) as the basic equation for our ternary full adder throughout the rest of this paper.

**DIRECT OPERATION ON TERNARY DELTA MODULATED SEQUENCES**

Delta modulation is a one-bit A/D conversion method, a ternary delta modulator transforms an analog input signal \(X(t)\) to a ternary sequence:

\[
X_n = \ldots X_{-1}, X_0, X_1 \ldots \ldots
\]

where \(X_i\) takes values +1, 0, or −1 at intervals of \(T\)-seconds. The feedback path of the system consists of an ideal integrator and an amplifier, much the same as in binary case. The impulse response of the ideal integrator will be a piece-wise linear function. The amplifier has a gain \(\delta\) causing the feedback slope size to be \(\delta\) also. The integrated feedback output signal \(X(t)\) is given by

\[
\hat{X}(nT) = T \cdot \delta \sum_{k=-\infty}^{n-1} x_k
\]
or
\[
\hat{X}(t) = T \cdot \delta \sum_{k=-\infty}^{n-1} x_k + (t - nT) \cdot \delta \cdot X_n
\] (5)

for \( nT \leq t \leq (n + 1)T \), it follows that

\[
X(t) = \hat{X}(t) + \epsilon_1(t)
\] (6)

where \( \epsilon_1(t) \) is the error signal introduced by the modulator.

In order to realize a digital filter based on ternary delta modulation, we should be able to operate the ternary delta modulated sequence directly (2). Again, since addition is the basic algorithm for digital signal processing, we now first consider how to form the sum of two ternary delta modulated sequences.

Assume that \( \{ X_n \} \) and \( \{ Y_n \} \) are the output sequences of identical ternary delta modulators which have analog inputs \( X(t) \) and \( Y(t) \), respectively, and which are controlled by the same clock generator. From the ternary full adder equation, we have

\[
S_n = \frac{1}{3} [ X_n + Y_n - (C_n - C_{n-1}) ]
\] (7)

This implies that the ternary full adders can be used to form the sum, \( \{ S_n \} \), of two ternary delta modulation sequences \( \{ X_n \} \) and \( \{ Y_n \} \). \( \{ S_n \} \) can be considered as the ternary delta modulation sequence of one third the sum of the analog signals \( X(t) \) and \( Y(t) \) with an error. For any \( k < n \), we have

\[
\sum_{n=k}^{N} S_n - \frac{1}{3} [ \sum_{n=k}^{N} X_n + \sum_{n=k}^{N} Y_n ] = \frac{1}{3} \sum_{n=k}^{N} (C_{n-1} - C_n) = \frac{1}{3} (c_{k-1} - c_N)
\] (8)

Since \( |C_n| < 1 \) for all \( n \), the absolute value of the left side of (8) will be bounded by \( 1/3 \cdot (1 + 1) = 2/3 \), i.e.

\[
\left| \sum_{n=k}^{N} S_n - \frac{1}{3} [ \sum_{n=k}^{N} X_n + \sum_{n=k}^{N} Y_n ] \right| \leq 2/3
\] (9)

and the estimate of \( S(t) \) will be

\[
\hat{S}(t) = \frac{1}{3} [ X(t) + Y(t) ] - \frac{1}{3} [ \epsilon_1(t) + \epsilon_2(t) ] + \varphi(t)
\] (10)

\[
\text{for } nT \leq t \leq (n + 1)T
\]

where

\[
|\varphi(t)| \leq 2/3 \delta \cdot T
\] (11)
\[ X(t) = \hat{X}(t) + \epsilon_1(t) \quad (12) \]
\[ Y(t) = \hat{Y}(t) + \epsilon_2(t) \quad (13) \]

The term \( 1/3 \left[ \epsilon_1(t) + \epsilon_2(t) \right] \) is one third the sum of errors of a delta modulation system whose input is the analog signal \( 1/3 \left[ x(t) + y(t) \right] \).

The error \( | \varphi(t) | \leq 2/3 \delta \cdot T \) can be reduced to any acceptable level by decreasing step size (i.e. increasing sampling frequency) such that \( \delta / T \) remains constant. The identical error bound holds for one third of the difference of two modulation systems.

In order to verify the practical possibility to directly operate on ternary delta modulated signal, a computer simulation model has been built as shown in Figure 2 where

\[ X(t) = -\sin(\omega t) + 0.5 \cos(2\omega t) \quad \text{and} \]
\[ Y(t) = 0.5 \cos(3\omega t) \]

\( X(t) \) and \( Y(t) \) are the outputs of ternary delta demodulators, respectively. Their sum is \( \hat{X}(t) + \hat{Y}(t) \). After processing ternary sequences, \( X_n \) and \( Y_n \), in ternary full adder and after ternary delta demodulation the sum is \( \hat{S}(t) \). The equivalent error is \( \epsilon(t) \). After low-pass filtering the revived signal is \( S(t) = 1/3 \left[ X(t) + Y(t) \right] \).

If there are 1 analog signals, \( X_1(t), X_2(t), \ldots, X_1(t) \), then we can use successive summing to determine the ternary delta modulation sequence of their sum, \( s(t) \), as shown in Figure 3. Thus,

\[ S(t) = \frac{1}{3^{r+1}} \left[ \sum_{i=1}^{l} x_i(t) \right] \quad (14) \]

where \( r \) is the positive integer, representing the times of successive groupings and satisfying

\[ 2^r < 1 < 2^{r+1}, \quad r = 1, 2, \ldots \quad (15) \]

Since the absolute error per summing step is bounded by \( 2/3\delta T \) as pointed out above in (8), therefore, the total error in \( r \) successive grouping (therefore \( r + 1 \) successive summings) is \( (2/3 \cdot \delta \cdot T) \cdot (r + 1) \). The successive grouping shown in Figure 3, for instance, has 3 summing steps (\( r = 2 \)) thus the absolute total error is less than \( (2/3 \cdot \delta \cdot T) \cdot (2 + 1) = 2\delta T \).
In binary case one of the great advantages in realization of digital filter based on delta modulation is multiplication-free. In ternary case we can replace multiplication of filter coefficient \( \alpha \) and input signal by successive application of the ternary addition operation, if \( \alpha \) is any non-zero constant of modulus < 1/2 for the following reason:

First let \( |\alpha| \) round-off to \( k \) significant ternary bits, we have

\[
|\alpha| = \frac{\alpha_1}{3} + \frac{\alpha_2}{3^2} + \ldots + \frac{\alpha_k}{3^k}
\]  

(16)

with each \( \alpha_i \ (1 < i < k-1) \) equal to +1, 0, or -1, and \( \alpha_k = +1 \) or -1.

Obviously,

\[
|\alpha| < \frac{1}{3} + \frac{1}{3^2} + \ldots + \frac{1}{3^k} + \ldots = 1/3 \cdot \frac{1}{1 - \frac{1}{3}} = 1/2
\]

(17)

Now \( \alpha X(t) \) can be written as follows,

\[
|\alpha| X(t) = (\alpha_1 X(t) + (\ldots (\alpha_{k-1} X(t) + (\alpha_k X(t)) 3^{-1} (3^{-1}) \ldots)) 3^{-1}
\]

(18)

The ternary delta modulation sequence, \( \{ P_n \} \), of the product \( \alpha X(t) \) can be determined by the following relation:

\[
\{ P_n \} = (B_n^{(1)}, (\ldots (B_n^{(k-1)}, (B_n^{(k)}, I_n)) \ldots)) \ldots)
\]

(19)

\[
\begin{align*}
B_n(i) &= X_n & \text{if } \alpha_i = 1, \\
B_n(i) &= -X_n & \text{if } \alpha_i = -1, \\
B_n(i) &= I_n & \text{if } \alpha_i = 0
\end{align*}
\]

(20)

where \( \{ I_n \} \) is the idling sequence defined as

\[
I_n = \ldots . I_{-1} I_0 I_1 \ldots \quad \text{with } I_n = -I_{n-1}
\]

(21)

\[
n = -1, 0, 1, \ldots \quad \text{and } I_i \text{ takes the value } +1, 0, \text{ or } -1.
\]

The total error \( \varphi(t) \) for the ternary delta modulation sequence \( \{ P_n \} \) satisfies

\[
\varphi(t) < \sum_{j=1}^{k} |G_j(t)| 3^{-(k-j)} \leq 2/3 \delta T \sum_{j=1}^{k} 3^{-(k-j)} = T \left( \frac{2}{3} \right) \delta \cdot \frac{1 - (\sqrt[3]{3})^k}{1 - (\sqrt[3]{3})} = \delta \left[ 1 - \left( \frac{1}{3} \right)^k \right] T \leq \delta T
\]

(22)
Since for each individual step, the error $|\varphi(t)| \leq (2/3) \delta T$. Thus $|\varphi(t)| \leq \delta T$ is independent of $k$, which gives a bound on the overall error $\delta(t)$. Therefore the realization of delta multiplier at the output of which a delta sequence of the product $\alpha X(t)$, \{ Pn \}, with $|\alpha| < 1/2$, can be obtained very easily. For example if we want to implement $\alpha X(t)$ where $\alpha$ is the ternary number, say, represented by $0.1\overline{1}0\overline{1}$, then the following arrangement will give us the delta sequence of $\alpha X(t)$. (see Figure 4) Where we need sign-conversion of input sequence, which, however, is very easy to implement in our ternary symmetric signed number system.

Figure 5 shows a tree of delta full adders for all ternary values of coefficients with $k = 2$. These coefficients are shown at the outputs of the delta full adders. A digital ternary multiplier can be used to select the output for various desired multiplication coefficients from the tree. Extension of the tree to the case where $k > 3$ is easily achieved. Thus multiplication of $x(t)$ by any filter coefficient $\alpha$ with $|\alpha| < 1/2$ can be realized.

**DIGITAL FILTER REALIZATION BASED ON TERNARY DELTA MODULATION**

The synthesis of digital filter with ternary delta modulated signal can also be stored in a one-ternary-bit memory element. Figure 6 gives the block diagram for a ternary delta modulation system. The ternary delta modulation sampling rate is also $k$ time the Nyquist frequency. The sampling frequency can be increased until the quantization noise is sufficiently small. An interpolator filter is usually placed at the output of a non-recursive digital filter. In the case of ternary delta modulation, this filter can also be a simple RC.

Ternary non-recursive filter is of a great interest in the filter realization based on ternary delta modulation. The transfer function of a non-recursive digital filter is

$$H (Z^{-1}) = \sum_{k=0}^{P} \alpha_k Z^{-k}$$

(23)

In terms of actual input and output delta modulation sequences, the output at the $n$-th stage is

$$Y_n = \sum_{k=0}^{P} \alpha_k X_{n-km}$$

(24)

where $m$ is the number of stages of each ternary shift register considered as a ternary unit delay.
From (24) and if the filter coefficient $\alpha_k$ does not absolutely exceed $\frac{1}{2}$, the realization of a ternary non-recursive digital filter is possible by use of a signal tree of ternary delta modulation full adders instead of multipliers as mentioned in last section. The output of this tree of delta full adders are forward to shift registers of 0, m, 2m ...... m stages. The output of these registers are then directly fed to a $(p + 1)$-input delta full adder, as shown in Fig. 7.

Care must be taken here because the output sequence of the digital filter is a delta modulation sequence of an analog signal divided by $3^{r+1}$ if

$$2^r \leq p + 1 \leq 2^{r+1}$$

(25)

for the reason described in previous section, since the sequence is taken from a $(p + 1)$-input delta adder. However, this signal attenuation may also be reduced in a non-recursive digital filter of the usual tapped delay line form as follows: First the coefficients of (24) may be written

$$\alpha_k = \gamma_k 3^{-1k} \quad k = 0, 1, .......

(26)

with $1/3 < \gamma_k < 1/2$ and $1k$ is a non-negative integer number. This is because we require the first significant digit after decimal in ternary number representation is non-zero and we require that the coefficients, $\alpha_k$ be absolutely less than $1/2$. The coefficients are then grouped as follows:

$$( \delta_1 3^{i-1}, \delta_2 3^{i-2}, ......., \delta_v 3^{i-v} )$$

(27)

with $i$ and $v$ non-negative integer numbers, and the coefficients $\delta_1, \delta_2, ......., \delta_v$ are members of the set of the coefficients $\gamma_0, \gamma_1, ......., \gamma_p$. Furthermore every coefficient with $1k = 0$ in (26) is taken alone as a group. With such coefficient grouping, the synthesis of Figure 8 can be formed, which supplies an output sequence with no attenuation. This method also can reduce considerably the total number of delta modulation full adders of a filter.

A ternary T gate has been constructed and it can be used as a basic building block to make both the combinatorial and sequential circuits. The ternary T gate is defined as

$$T(p,1,r,s) = p J_1 (s) + q J_0 (s) + r J_{-1} (s)$$

(28)

where the variables are $p, 1, r$ and $s \{ +1, 0, -1 \}$ and where the product $\bullet$, the sum $+$ and $J$ operations are defined as follows:
\[ x \cdot y = \min (x, y), \quad x + y = \max (x, y) \]

\[ J_k(s) = \begin{cases} 
+1 & \text{for } s = k \\
-1 & \text{for } s \neq k
\end{cases} \]

A practical realization of the T gate has been given (5) (6). Physically a T-gate is a 4-input gate the output of which assumes the values of p, q, or r, according to the value of s. Thus s is called a control signal on the T-gate.

A ternary full adder which has the truth table as shown in TABLE 1 can be realized by using such universal T gates, since the sum \( S(X_n, Y_n, C_{n-1}) \) and the carry \( C(X_n, Y_n, C_{n-1}) \) of ternary delta full adder can be addressed by 14 T gates as follows:

\[
S(X_n, Y_n, C_{n-1}) = T(T(0, -1, 1; X_n), T(-1, 1, 0; X_n), X_n;
T(Y_n, T(0, -1, 1; Y_n), T(-1, 1, 0; Y_n); C_{n-1})
\]

\[
S(X_n, Y_n, C_{n-1}) = T(T(1, 1, 0; X_n), T(1, 0, 0; X_n), 0; Y_n;
T(T(1, 0, 0; X_n), 0, T(0, 0, -1; X_n); X_n),
T(0, T(0, 0, -1; X_n), T(0, 1,-1; X_n); Y_n); C_{n-1})
\] (29)

The T gate can be used not only as the switching gate but also as the ternary storage element. A tristable multivibrator is constructed by using the T gate as a basic building block. Tristable state \( x = +1, 0, \) and -1 can be obtained directly by \( T(+1, 0, -1; x) = x. \) The tristable multivibrator has a function analogous to the binary D-flip-flop. Cross-coupling two T gates we obtain a tristable multivibrator(7).

With available ternary full-adders and ternary shift registers (DFFF) we can complete, implementation of digital filter by the method developed in reference(2)(4). A block diagram of filter realization is shown in Figure 9.

**CONCLUSION**

We have shown the possibility of direct operations on ternary delta modulated digital streams by mathematical deduction. With the existing universal T gates, we also present the hardware implementation of ternary full adder and multiplier, which leads to a new realization of non-recursive digital filters based on ternary logic and ternary delta modulation. The primary advantage of the ternary scheme is the simplicity of the hardware and the reduction of the number of interconnections and the number of gates when the chip is produced in VLSI environment. These ideas can be extended to recursive digital filter and applied to digital signal processing in general.
REFERENCES


![Figure 1 - Ternary Full Adder](image1.png)

![Figure 2 - Block Diagram Of Simulation Model](image2.png)
Figure 3 Successive Grouping

Figure 4. Multiplication by a Ternary Constant

Figure 5. Tree of Ternary Full Adders for all Coefficients with Two Ternary Bits
Figure 6  Ternary Delta Modulation System

Figure 7. Non Recursive Ternary Filter with a Tree of Ternary Adders

Figure 8. Arrangement for Output with no attenuation
Figure 9 Arrangement of nonrecursive DF

<table>
<thead>
<tr>
<th>TABLE 1. TERNARY ADDER TRUTH TABLE (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_N )</td>
</tr>
<tr>
<td>( S_N )</td>
</tr>
<tr>
<td>( C_N )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE 2. TERNARY ADDER TRUTH TABLE (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_N )</td>
</tr>
<tr>
<td>( S_N )</td>
</tr>
<tr>
<td>( C_N )</td>
</tr>
</tbody>
</table>