ABSTRACT

A review is presented of some new, low-cost, easy-to-use hardware for interfacing small-scale digital systems to telecommunications and data link networks. Devices featured are binary serial interfaces, protocol controllers (including SDLC and HDLC), data encryption units (including the new NBS Federal Standard), modems, and information encoders. Compatibility with existing microprocessors and future trends are discussed.

INTRODUCTION

With the advent of large-scale integrated circuits (LSI) and microprocessors (μP), mankind’s dream of universal, instant personal communications seems about to be realized. In the meantime, the presently available LSI chips can greatly simplify the task of providing remote data links for products in the home, factory, and laboratory. Many of the complex interface functions normally performed by elaborate, tailor-made circuit boards have now been condensed onto single, easy-to-use, and inexpensive IC chips. The detailed software needed to implement the increasingly elaborate data link control protocols and standards can likewise be replaced by pre-programmed LSI peripheral chips capable of being configured by a few software instructions. Interesting design tradeoffs confront the communications engineer; for example, automatic dialup can be accomplished either by using software timing loops or on-board timers (such as contained on the Intel 8048, Mostek 3870, or Motorola 6801 single-chip microprocessors), or by means of LSI telephone dialer chips (such as the Mostek 5090).

LSI communications interface chips generally attach directly to the μP data, address, and control buses and operate either as input-output ports (as in the Intel μP architecture) or as memory locations (such as in the Motorola μP architecture). The software overhead required by the system μP to configure peripheral chips consists of a few IN and OUT or
LOAD and STORE instructions. Once programmed, these interface devices can automatically send and receive blocks of data for the CPU in polling or interrupt modes or by communicating directly with system memory via the direct memory access (DMA) mode.

The present article features some representative LSI devices now available at low-cost (less than $30) and high volume. For more complete tabulations and further technical information, the reader is referred to several recent review articles (Refs. 1-3). For additional material on modern data link and line control protocols and standards see Refs. 3-5.

**BINARY SERIAL INTERFACES**

The parallel µP data bus may be interfaced to the serial communication channel by means of programmable asynchronous or synchronous receiver-transmitter chips known as USARTs. An example is the Signetics 2651 Programmable Communications Interface (PCI), designed to attach directly to the Signetics 2650 µP bus lines. Use of this IC to implement a telecommunications data link is shown in Fig. 1.

Serial data is received and transmitted on pins RXD and TXD and synchronized by clock inputs RXC and TXC (up to 800 Kb/s). For asynchronous transmission, timing is derived from an on-board baud-rate generator (up to 19.2 Kb/s). A standard RS232C modem is interfaced via control lines RTS, CTS, DCD, DSR, and DTR. Parallel data flows to and from the CPU via the µP data bus. The LSI device functions by storing parallel data in holding registers and shifting the bits one at a time to and from the serial communications line with shift registers. Start and stop bits are automatically inserted and deleted. The PSI is programmed by writing data into the 3 on-board control registers, whose bits specify mode (asynchronous or synchronous), clock rate; character length (5-8 bits); parity, number of stop bits (1, 1.5, or 2), modem transmit control, reset option, and echo or loopback operating mode. Data integrity is checked by reading the status register bits representing: holding buffers full flags, modem receive flags, framing and synch errors, parity error overrun errors. Provisions are also made to allow non-ASCII user data (transparent data encoding) to be mixed with standard ASCII synch characters in an unambiguous fashion.

**DATA LINK CONTROLLERS**

The earlier byte-oriented data communications protocols such as IBM BISYNC and DEC DDCMP are now being supplanted by the more straightforward and versatile bit-oriented protocols such as IBM SDLC, ANSI ADCCP, and ISO HDLC. Data link control (DLC) chips have been developed to automate the framing, checking, and acknowledging of
formatted data blocks (Fig. 2) during high-speed synchronous transmission. One typical
device is the Motorola MG6854 Advanced Data Link Controller (ADLC) chip, designed
to attach to M6800 µP bus lines. The ADLC device implements the ADCCP, HDLC, and
SDLC standard bit-oriented protocols. Opening and closing SYNCH flags (0111 1110) are
automatically inserted and deleted. Address, control, and logical fields may be extended by
the user. The device also includes a binary serial interface of the type described in the
previous section. Automatic frame checking is performed according to the CCITT-CRC
error detection schemes. Transparent (non-ASCII) user codes may be used without
confusion with framing flags by an automatic zero insertion and deletion procedure. FIFO
stacks of buffer registers are provided for storage of received data to expedite aknowledge
and retransmit protocols and to prevent overrun (pileup) of input data. In addition to the
receiver and transmitter registers, there are two status registers and four control registers
used for configuring and programming the ADLC and checking data. Manipulation of
status and control bits allows handshaking with RS232C modems, DMA block transfers;
polling, loop, and test operation modes; and word length selection. The MG6854 ADLC
chip can provide data rates up to 660 Kb/s.

DATA ENCRYPTION UNITS

Increased concern over computer privacy and security (Ref. 6) has stimulated the adoption
of the Federal Data Encryption Standard (DES) developed for NBS by IBM. This
encryption algorithm employs a 56 bit user-provided key, arranged as 8 bytes of odd
parity data, which is then merged with 8 bytes of cleartext to form 8 bytes of ciphertext. The
decryption scheme uses the same key and algorithm to invert the ciphertext. One LSI
implementation of the DES is the Intel 8294 Data Encryption Unit (DEU) chip. The device
attaches directly to the Intel 8080 or 8085 µP bus and is treated in software as an I/O port.
In the control mode (odd port address) the following commands may be written into the
control register: enter new key, put device in encrypt mode, put device in decrypt mode,
configure interrupt and DMA lines, and set 7 output pins for user-prescribed handshaking
with peripherals. Status register data may be read out to check: key parity error,
handshake flag, decrypt/encrypt mode, and data buffer full flags. In the data mode (even
port address) input and output bytes are processed and stored for later handling by the µ P.
The 8294 DEU may be operated at data rates of 150 bytes/sec, and is suitable for low-
speed (up to 1200 bps) telecommunications channels. For increased security, data stored in
the key register cannot be read onto the data bus.

CODECS AND MODEMS

Two other new LSI chips are useful for operating a high-speed data channel. Digital
telephone systems can be implemented via the Signetics ST100 coder/decoder (codec),
which is a companding a/d converter. Each analog voice-band waveform is sampled at
8 kHz and converted into a series of 8 digital bits according to the µ-law or A-law compression algorithms. Serial digital data (PCM) is transmitted, received, and converted at up to 2Mb/s using pairs of codecs.

Various LSI modulator-demodulators ( modems ) are also available including the Motorola M6860 low-speed (0-600 bps) modem. The device attaches to the M6800 µP bus and is capable of interfacing a digital bit stream with a series of precision sine wave segments via frequency-shift keying (FSK), where the binary 1 state is represented by 1270 Hz and the binary 0 state is represented by 1070 Hz in the originate mode. RS 232C handshake protocols and numerous other user and self-test options may be selected by applying 0 or 5 volts to the appropriate package pins. Higher speed phase shift keyed (PSK) modems are also available in LSI form from Motorola.

FUTURE TRENDS

It is safe to project LSI technology moving toward lower cost, higher speed, lower power, and higher density. Higher density (VLSI) means more functions on each chip and “smarter” chips (e.g., the Intel 8022 µP contains a complete microcomputer including a/d converter on a single chip). Eventually LSI data link chips may include modems, dial pulse and tone generators, codecs, and µP thrown in for free. LSI technology may soon embrace multiplexors, concentrators, packet-switching, message-switching, and time-division-switching. Implementation of these devices will require hybrid technology (digital and analog circuits on the same substrate). Higher-density program memory means easier-to-use, higher-level software and more comprehensive system resources. The development of bubble memories capable of storing 1 Mb/sq. in. permits local systems with large user data bases such as phone directories and code books.

The DEU chips now available require the distribution and safeguarding of random cipher keys for both sender and receiver. A more efficient procedure is embodied in the new “trap-door” ciphers (Ref. 7) for which the encryption keys can be published openly and only the decrypting keys need be secured. LSI devices implementing these trap-door encryption algorithms are now being developed at MIT and Stanford.

REFERENCES


Fig. 1 Synchronous Interface to Telephone Lines Using the Signetics 2651 PCI (from Ref. 3)
<table>
<thead>
<tr>
<th>01111110</th>
<th>8 bits PER BYTE</th>
<th>8 bits PER BYTE</th>
<th>8 bits PER BYTE</th>
<th>VARIABLE LENGTH (5-8)</th>
<th>16 bit</th>
<th>01111110</th>
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<tr>
<td>(opening)</td>
<td>ADDRESS² FIELD</td>
<td>CONTROL² FIELD</td>
<td>LOGICAL CONTROL</td>
<td>FRAME CHECK</td>
<td>SUB-FIELD (option)</td>
<td>SEQUENCE FIELD</td>
</tr>
<tr>
<td>EXTENDABLE (optional)</td>
<td>INFORMATION FIELD</td>
<td></td>
<td></td>
<td></td>
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Fig. 2 - Data Format of a Frame