A MULTICHANNEL DATA ACQUISITION SYSTEM 
BASED ON PARALLEL PROCESSOR ARCHITECTURES

B. GELHAAR, K. ALVERMANN, F. DZAAN

DLR
German Aerospace Research Establishment
Institute For Flight Mechanics
Braunschweig, FRG

1. KEY WORDS

Parallel Processing, Transputer, Delta Sigma Converter, Data Acquisition

2. ABSTRACT

For research purposes on helicopter rotor acoustics a large data acquisition system called TEDAS (Transputer based Expandable Data Acquisition System) has been developed. The key features of this system are: unlimited expandability and sum data rate, local storage of data during operation, very simple analog anti aliasing filtering due to extensive digital filtering, and integrated computational power which scales with the number of channels. The sample rate is up to 50 kHz/channel, the resolution is 16 bit, 360 channels are realized now.

TEDAS consists of blocks with 8 A/D converters which are controlled by one transputer T800. The size of the local memory is 4 Mbyte. Any number of blocks (IDAM = Intelligent Data Acquisition Module) can be combined to a complete system. Data preprocessing is done in parallel inside the IDAMs. As for 16 bit systems the analog antialiasing filtering becomes a dominant factor of the costs, delta sigma ADCs with oversampling and internal digital filtering are used. This produces an exact linear phase and a stop band rejection of -90 dB.

3. THE APPLICATION

Helicopters are noisy vehicles. In addition they have bad comfort because of strong vibrations. Therefore, one of the objectives of helicopter research is the reduction of noise and vibration by having a deeper understanding of the airflow. This can be achieved by measurement of the aerodynamic effects of the rotor in wind tunnels. For the Cp-Rot project [1], 124 pressure sensors, 75 strain gauges and some temperature sensors win be
fitted inside the blades of a model helicopter rotor; Fig. 1 gives an overview over the entire measurement system. According to the large number of sensors, a high sample rate is necessary to provide a high resolution in time of the instationary airfoil surface pressure data.

4. THE MEASUREMENT TASK

4.1. DATA ACQUISITION

The sensor signals are amplified by a signal conditioning unit which is placed on the top of the rotor as part of the rotating system. The analog signals then are transferred by a slip ring into the inertial system where the A/D conversion is performed. The rotor rotates at
17.5 Hz. A/D conversion is required at a rate of 2048 points per rotation or 35840 Hz. One measurement cycle covers 100 rotations. There are 180 channels and this results in

2048 samples/rotation x 100 rotations x 180 channels = 36,864,000 samples

per measurement. The wordrate per channel is

17.5 x 2048 words/s = 35840 words/s.

producing a sum word rate of 180x35840 = 6,451,200 words/s. Assuming 2 byte/word data has to be stored at 12,901,400 byte/s.

4.2. DATA PROCESSING

A lot of data processing has to be done on the measured raw data. In detail the following has to be performed for each of the 180 channels:

1. FFT about the 2048 points of each rotation of the rotor.
2. Average of the FFT’s of all 100 rotations.
3. Time domain average of all 100 rotations.
4. RMS (Root Mean Square) value of all data of all rotations.
5. Complex product of the averaged FFT data of one selected channel, called the reference channel, with the averaged FFT data of all other channels.

The raw data and processed data then give the complete data set for one measurement which will be distributed to other institutions for further evaluation. In sum

180x100 = 18000 FFTs (with 2048 points), and 180x1024 complex products

and several averaging and other computations have to be performed for one shot. Data preprocessing and storage is done local on an IDAM basis before raw data and preprocessed data is sent to a host computer with a mass storage device.

5. A/D CONVERTERS

Three techniques have traditionally been used for the implementation of A/D converters: successive approximation converters, counting converters and flash converters. All these techniques sample the input considering the Nyquist criterion (sampling rate at least twice the highest input frequency). All these techniques need extremely high performance antialiasing filtering and sample & hold circuits to ensure better than 12 bit accuracy. Since several years a rather old technology becomes more important especially in audio
signal processing: DELTA SIGMA ADCs. This rediscovered technology which integrates analog and digital functions on one chip now allows low cost high performance A/D conversion by mapping most of the required analog functions into the digital domain. The delta sigma modulator (Fig. 2) itself is the only analog part of the ADC and only requires 10 percent of the die area [2].

5.1. DELTA SIGMA CONVERTERS

5.1.1. Oversampling and anti-aliasing filtering

Delta sigma converters are using a high degree of oversampling combined with a low resolution 1 bit A/D converter. Used oversampling factors are 64 to 256. By oversampling an input signal, the requirements directed to the analog anti-aliasing filter reduces dramatically. The sampling mechanism effects the spectrum of an analog signal. A continuous signal \( U_a \) is sampled by getting probes of it at equidistant points of time \( t_n = nT_s \) (Fig. 3). Then the original function is replaced by a set of Dirac pulses at each \( t_n \). The size of the pulses (not the height, because Dirac pulses have per definition infinite height and infinitely small width, with known area) equals the value of the original function at \( t_n \). The sampled version of \( U_a \) gives

\[
(U_a)_{\text{samp}} = \sum_{n=0}^{\infty} U_a(t_n) T_s \delta(t-t_n)
\]

The spectrum of this function can be expressed using the Fourier transformation:

\[
(U_a)_{\text{samp}}(j, \omega) = T_s \sum_{n=0}^{\infty} U_a(nT_s) \exp(-2\pi j \omega n)
\]

with \( f_s \) called the sampling frequency. As one can see, this spectrum is periodic in \( f_s \) (Fig. 4).
All parts of the spectrum at frequencies greater than \( f_s/2 \) have to be removed later after final D/A conversion by an analog output low pass filter. If the spectrum of the original function \( U_a(t) \) has nonzero components at frequencies greater than \( f_s/2 \) or if the sampling frequency \( f_s \) is lower than twice the highest frequency contained in the original time domain function, disturbing aliasing effects take place (Fig. 5). This means that parts of the spectrum outside the band of interest are mapped into the band of interest (Fig. 6).

Therefore, before sampling, the input signal has to be bandlimited by an analog low pass filter with the stop band starting at least at \( f_s/2 \) (Fig. 7).

On the other hand one tries to hold the sampling frequency \( f_s \) as low as possible because of the cost of fast A/D converters. So an ideal filter would be required with a transfer function

\[
F_{\text{filter}} = 1 \quad \text{for input frequencies between 0 and } f_s/2, \\
F_{\text{filter}} << 1 \quad \text{for input frequencies } > f_s/2.
\]

Of course such a filter is not possible, especially in time domain. High order analog antialiasing filters can produce small transition bands between pass band and stop band but have either great ripple in the pass band or great phase nonlinearities (\( \text{d} \phi / \text{d} \theta \) not constant). One solution for this problem would be to make \( f_s \) very great in order to realize the antialiasing filter with a very simple RC lowpass filter, which doesn’t introduce significant
phase distortion for frequencies of interest but produces enough rolloff for frequencies up to \( f_s/2 \) which is far away from the band of interest (Fig. 8). This is called oversampling.

Oversampling needs no or at least very simple analog antialiasing filters, but on the other hand requires very fast A/D converters and produces very high output wordrates producing an output band in digital domain which is very much greater then the band of interest and therefore very hard to handle during the following signal processing steps. For a required output wordrate \( f_w \) of 50 KHz, oversampling by 64, results in a sampling rate \( f_s = 64 \times 50 \text{ KHz} = 3.2 \text{ MHz} \). On the other hand the requirement for the analog antialiasing filter now reduces dramatically to:

\[
\begin{align*}
F_{\text{filter}} &= 1 & \text{for } 0 > f_{\text{in}} > f_w/2 = 25 \text{ KHz (the band of interest)}, \\
F_{\text{filter}} &<< 1 & \text{for } f_{\text{in}} \geq f_s/2 = 1.6 \text{ MHz}.
\end{align*}
\]

This can be achieved using very simple RC lowpass filters. But the problem is, that we get data at \( f_s \), instead of the required wordrate \( f_w \). The process to reduce the number of words to compute is called decimation. It takes place by filtering the digital information in digital domain by a lowpath filter with corner frequency \( f_c = f_w/2 = f_s/64 \) (for this example). By doing this, the frequency components

\[
f_c < f < f_s
\]

are removed. Components in the area

\[
f = nf_s \pm f_c \quad (n = 0,1,2,3...)
\]

are not removed but can be rejected easily by analog output filtering after final D/A conversion (Fig. 9, 10, 11). Because the cut frequency of the digital filter \( f_c = f_s/64 \) it is allowed to pick every 64th value of the output of the filter without violating the sampling theorem. Note that the spectrum of the signal after decimation is periodic in \( f_s/64 \) because decimation is a sampling process too.

5.1.2. Delta sigma modulator

The process of sampling and A/D conversion is done by a circuit consisting of four major elements:

1. Sample & hold,
2. Integrator or lowpass filter,
3. Comparator,
4. D/A converter (1 bit),
arranged in a closed loop scheme (Fig. 2). The shown delta sigma modulator in the simplified diagram is a first order modulator or a simple voltage to frequency converter. The order of a delta sigma modulator indicates the order of analog filtering or integration in the loop. The output of the first order modulator is a stream of bits producing a one or a zero for each clock cycle at \( f_c \). The average of the 1 bit information delivered at the high frequency \( f_s \) represents the input voltage. This could be the input of a counter averaging the bits over \( 2^n \) cycles giving an output with the resolution of \( n \) bits. Using 3rd or 4th order modulator and doing sophisticated FIR low pass filtering of the output instead of simple counting allows an output of \( n \) bit resolution after dramatically fewer samples than \( 2^n \).

Fig. 12 shows the structure of a todays 4th order modulator [3].

The advantage of the 1 bit quantizer is that errors in the 1 bit feedback DAC do not produce distortion but only gain and offset errors [4].
5.1.3. Quantization noise

The 1 bit modulator produces much quantization noise. The signal to noise ratio of a n bit ADC is given by

\[ S = n \times 6 \text{ dB} + 1.8 \text{ dB}, \text{i.e.} \]
\[ 7.8 \text{ dB for } n = 1 \] [5].

The RMS of the noise is \( U_{\text{LSB}}\sqrt{12} \). But only a fraction of the noise energy resides in the band of interest as the noise is spread over a wide area of frequency. Nevertheless further reduction of quantization noise is required in order to get a high range of dynamic. Looking at an analog model of the modulator and introducing a noise source \( P(n) \) (Fig. 13) representing the nonlinear comparator function, allows to give an assessment about the quantization noise.

---

**Figure 12:** Fourth order delta sigma modulator

**Figure 13:** Noise model of a delta sigma modulator
The transfer function $H(f)$ describes the analog integrator of any order. Assuming $D_m = 0$ gives:

$$D_{\text{out}} = P(n) @ H(f) \cdot D_{\text{out}} = P(n) / (1 + H(f))$$

Thus, the quantization noise at the output is function of $H(f)$. If $H(f)$ is large at low frequencies (i.e. for the frequencies of interest), the quantization noise for this frequencies is reduced. As $H(f)$ become smaller for higher frequencies (in the area of frequencies not of interest) the noise increases in that area. This is because the noise is added directly to the output and, therefore, only the noise distribution but not the noise energy in total is affected by the closed loop circuit. Fig. 14 shows the simulated output spectrum of a modulator [3]. It is necessary to filter the output sequence of the modulator in order to remove all frequency components which are outside the band of interest.

![Figure 14: Simulated output spectrum of a delta sigma modulator](image)

6. DIGITAL FILTERING AND DECIMATION

The digital filter is a very important component of a delta sigma ADC. Just the filter allows further reduction of the word rate (decimation), remove of all disturbing noise, the modulator produces and, therefore, production of high resolution outputs. Because of their strictly constant group delay ($d\varphi/dT = \text{constant}$) and easy implementation finite impulse response filters (FIR filters) are used. The output of a FIR filter is the convolution of a series of coefficients and an input series[6, 7]). In time domain the coefficients represent the answer of the filter at equidistant points of time for a Dirac impulse at the input. The output of the filter for a input sequence is given by the sum of products:
with \( x \) the filter input, \( y \) the filter output, the filter coefficients \( h(l) \) and \( K \) the number of filter coefficients.

The frequency response is given by:

\[
|H(e^{j\omega})| = \sum_{l=0}^{K-1} a(l) \cos(\omega l)
\]

with

\[
a(0) = h((K-l)/2) \quad \text{and} \quad a(l) = 2h((K-l)/2-l) \quad \text{for} \quad l = 1...(K-1)/2
\]

and

\[
h(l) = l\text{th coefficient of the filter.}
\]

The delay of such a FIR filter is \( n/2 \). If the filter sequence has a higher resolution in time than the coefficient series (more than one coefficient per input value) it is also possible to calculate output values which belong to a point of time between two values of the input sequence, which is very important for interpolation applications. This is done by shifting the input series in fractions of the distance between two samples.

If the filter is designed such that frequencies above, for example, a tenth of frequency of the input sequence are attenuated, then it is allowed to pick up only every tenth output of the filter for further processing without violating the Nyquist criterion. This process of reducing the word rate to a handable value is called decimation. This happens inside the A/D converters FIR filter in order to perform a bridge between the highly oversampling modulator and adequate word rates at the output of the converter. Actual delta sigma converter designs use FIR filters combined of several stages [8].

7. SYNCHRONIZATION

One of the problems of using delta sigma converters is that they have to run continuously. Unlike other converter technologies, which use a kind of start stop operation, delta sigma converters have their own time grid, which normally is derived from a crystal oscillator. This is no problem for audio or control purposes, because this oscillator can function as the main clock of the system which then run synchronously to this main clock.

The rotor acoustic measurement in opposite has to be synchronized to the rotor speed which is never constant because of the hydraulic motor and the aerodynamic forces. Because of FFT processing it is necessary to have a word rate of exactly 2048/rev. (per revolution). This gives a word rate of 35,840 kHz at the nominal rotor speed of 17.5 rev/s. The internal sample frequency of the ADC is \( 35,840 \times 17.5 \approx 2.3 \) MHZ. This frequency is
derivated from a PLL which multiplies the pulses from a shaft encoder by a factor of 4 (Fig. 15). Additionally the ADC needs six clock periods for every internal sample. These pulses are needed for internal filter computation and housekeeping purposes. They have not to be equidistant. Therefore, for each period of the PLL output a burst of six pulses is produced using a series of monoflops. The input frequency of the ADC results in \( \approx 13.8 \) MHZ. The reason for not using a higher PLL factor is that large PLL factors produce large phase distortion (jitter) which results in conversion errors (side lobes in the spectrum).

\[ \text{Figure 15: Synchronisation scheme} \]

8. TRANSPUTERS AND OCCAM

What we need for TEDAS is the massive use of parallel processing. The processing units are “Transputers” and they are programmed in the programming language OCCAM. Transputers are Von-Neummann-processors, each having its own memory. A transputer has four bidirectional serial links. These links enable it to exchange data with other transputers. By “linking” several transputers we get a transputer network. The single transputers in this network are working in parallel and asynchronous, there is no “master” or “supervising operating system”. The transputers synchronize their work by exchanging data.

We use the transputer T800 which has the following technical data. The T800 has (as a single processor) a performance of 10-15 MIPS / 2.0 MFLOPS (the T800 has a built-in floating point unit). It has 4 Kb of on-chip-memory, the TEDAS modules having 4 MByte of external memory. Each of the four links works with its own link engine at a data rate of 20 MBit per second in every direction (both to and from the transputer). In this way communication along the four links and calculation in the CPU are done in parallel. If we specify parallel processes on a single transputer, task switching is done in hardware and, therefore, very fast (a few microseconds).

Several transputers may be connected via their links in any way. This allows the mapping of the physical problem onto an appropriate network of processes (see e.g. [11]). Transputers were developed according to the concept of the programming language OCCAM. The basic element of OCCAM is a process. A process is an assignment (i.e. “a:=b+c”), a communication (i.e. “receive data from” or “send data to”) or a combination of other processes. Apart from usual constructs (such as “if”, “while” and so on),
processes may be combined in three principal ways: sequential, parallel and alternative. Sequential processes are executed one after the other, just as usual. Parallel processes are executed in parallel. As mentioned above, even processes on one transputer may work in parallel (i.e. communication and calculation). Processes are ideally working with their local memory and communicate via channels. Processes are synchronized by data transfer along these channels. An output process is waiting until all specified data is sent and then is terminated. An input process is waiting until all specified data is received and then is terminated. If an input/output process has to wait, it is (of course) descheduled by the hardware of the transputer, such that other (parallel) processes (on the same transputer) may be executed.

A complete program is placed by mapping processes on transputers and channels on the hardware links. This is done in a configuration part. If we change the hardware (by adding transputers to speed up the system), we only have to change the configuration data. Usually a transputer network is connected to a host computer. For TEDAS a SUN workstation is used. In the special case of the SUN, the host and the network are communicating along a link or with the help of shared memory.

9. SYSTEM DESCRIPTION

9.1. HARDWARE LAYOUT

Fig. 16 shows the structure of the complete data acquisition system. An unlimited number of Intelligent Data Acquisition Modules (IDAM’s) is arranged in a pipeline structure. Each module can serve 8 channels and is able to store 200,000 samples per channel. The sampling rate per channel is max. 50 KHz. After all modules have converted and stored the data from the rotor sensors for about 100 rotations, each module processes the data for its 8 channels.

After this is done, all raw data and processed data are transferred to a host computer where the data are stored on a mass storage device. The modules are connected via 20 Mbit/s transputer links. Also the connection to the host computer is made by a transputer link. The host computer can be any type for which a bus bridge head is available (VME-Bus, Q-Bus, PC-Bus and others). The actual system has been developed using a PC compatible host. The target system which, has been delivered to the customer, uses a SUN workstation as host. All the transputers in the IDAM’s are booted automatically via their links from the host. Of course there is a synchronization line which allows totally synchronous operation of all A/D converters. A special interface card provides clock data derived from the encoder which is mounted at the rotor shaft.
9.2. INTELLIGENT DATA ACQUISITION MODULE (IDAM)

Fig. 17 shows a block diagram of one IDAM. For the ADC the CS5329 from Crystal has been selected. It is operated in the testmode 6 [9] which allows operation at frequencies far away from the audio ADC values (44 or 48 KHz). In this testmode a built-in PLL is switched off, allowing to run the device outside the capture range of the PLL. The A/D converters deliver their data to an output registered shift register which can be read by the transputer under software control. The IDAM is a EURO long board which contains smaller modules i.e. the transputer module and two ADC modules. Fig 18 shows a FFT plot for the CS5329. Delta sigma converters have unlike converters no mechanism to produce systematic differential nonlinearity error. Fig. 18 also shows a DNL plot [10].

9.3. SOFTWARE LAYOUT

The IDAM’s are connected in a long pipeline. The first module is connected to the host, the last module has no successor. To simplify speech, we call the direction to the host “downstream”, the direction from the host to the last IDAM “upstream”. Two consecutive IDAM’s are connected by one link.
Figure 17: Structure of an IDAM

Figure 18: FFT and DNL plots of CS5329
Apart from the first IDAM, we execute the same process on all modules. The first IDAM has special hardware to start and end the data recording.

The communication works as follows. In normal state, the process on the IDAM is waiting for data coming upstream or downstream. If data is coming downstream, it is handed through to the predecessor, since all data going downstream is directed to the host. If data is coming upstream, a header tells the process, where it is directed. The data (or command) may be directed to all IDAM’s (e.g. “to all IDAM’s: initialize your AD converter”). The data may also be directed to a special IDAM (e.g. “to IDAM no. 13: send your FFT data”). If the data is meant for the process it is executed, otherwise it is sent further upstream.

We may set parameters in one or all IDAMs, convert the analog data and execute FFT’s or other transformation on the received data. In the end the host can request the processed data from the single IDAMs. There is a lot of data to be sent, the system transfers up to 800 Kb per second (transfer becoming slower, if the sending IDAM is farther upstream). In this way, the transfer bottleneck will be the harddisk on the host.

If a measurement is to start, the IDAM’s are initialized and change into a waiting status. No data may be transferred now. If all IDAM’s are ready, the first IDAM issues a hardware signal, such that all IDAM’s start their measurement at the same time. A measurement may be terminated by the host, but it is usually terminated when the specified amount of data is received. The process then returns to his normal state and the host may issue commands to process the raw data.

The data may be processed by an FFT, by averaging it in time, by calculating an RMS value, and other calculations. This should be the fastest way to preprocess the raw data, since it is done in parallel. If desired other preprocessing algorithms may be programmed.

In the end the host may request the raw data and/or the processed data. A SUN-SPARC Fileserver 370 stores the incoming data. The SCSI Harddisks can hold up to 2 GByte data, that can be copied to Exabyte-tapes and mailed to other institutions for further processing.

The SUN is equipped with the UNIX-based multiuser and multitasking operation system SUN OS 4.1. The application is based on OpenLook and X11/NeWS. X11/NeWS is a network based window-server, OpenLook is an intuitive grafical user interface.

The main duty of the application is to communicate with the transputer network which can be done on two ways: via a link adaptor, connected to the rootlink, performing an 8 bit parallel to serial conversion, and via VME-Bus with direct access to the entire dual ported memory of the root transputer. Normally, control commands are send to and acknowledgements are received from the network using the link adaptor. The incoming measurement data is received using the second way because of faster access to the data. Writing 70 MByte, a transfer rate of over 450 Kbyte/s is reached, hence the total data transfer takes about 2.5 minutes.

Finally, other programs in the workstation network may perform offline postprocessing such like extracting channels or displaying data.
In the current application, TEDAS handles 180 data channels. Calculating the 18000 FFT's (800 FFT’s per IDAM) will take about 3 minutes. The sending of all raw data (70 MByte) to the host and saving the data on a harddisk will take about 2.5 minutes (we can at most save 450 Kbyte per second on the harddisk).

10. CONCLUSIONS

As far as first tests showed, the highly oversampling delta sigma technology is not only usable for audio purposes, for which it was designed, but also for technical data acquisition problems. Mapping functions from the analog domain to the digital domain has the great advantage that the problem of noise introduction into high resolution converters can be maintained easily by digital filtering. The use of transputers in combination with OCCAM resulted in very modular easy to interface structure of the system. Adding more channels to the system is done by one connector ond the hardware side and the change of one parameter in software. As the CPU power is an integral part of the ADCs the preprocessing time is independent of the number of channels. Temporarily the fifth system of this type is being produced.

11. REFERENCES

[10] Analog/Digital Conversion ICs Data Book VOL 1, Crystal Semiconductor Corp. 1990