MULTISTATE ANALOG AND DIGITAL INTEGRATED CIRCUITS

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Summary. Several independent physical phenomena in unipolar and bipolar semiconductor pn junction devices and integrated structures lead to voltage and current-controlled negative resistance without the use of external feedback. These include avalanche breakdown, quantum mechanical tunneling, and minority carrier storage. Two complementary types of negative resistances may be utilized as a basis for generating multistable energy levels. The number of stable states and their relative spacings can be readily varied. Without negative resistance interaction, M+1 stable states can be generated where M is the number of negative resistance devices involved. With negative resistance interactions, additional multistability occurs, resulting in a total number of \((M+1) + (M-1)!\) stable states. S-S, N-N, and S-N interactions are analyzed. In the latter case, complementary negative resistances can be made to annihilate each other. Multistate tunnel and avalanche negative resistances have been made to occur in single devices resulting in tristable, quadristable and higher order energy levels. Variable radix counters, oscillators, frequency dividers, and high density memory elements have been fabricated both as hybrid and monolithic integrated circuits.

Introduction. The memory or store of a digital computer must be both accessible and erasable. The former implies that information can be located in the memory and extracted so that new information can be stored. Erasure of information in the store makes room for the admission of new data. The capacity of a memory is generally determined by the total number of binary digits, or words of a given number of binary digits that can be stored. Increased emphasis that has been placed on more efficient storage methods has been directed primarily toward materials research and size reduction through the use of integrated circuit technology.

Semiconductor memories are already being widely used for read-only random access and scratch pad applications and may be expected to be a potential candidate for the main frame computer organization. In many high speed and low power applications, semiconductor memories are replacing their magnetic counterparts. The current trend in semiconductor memories is to put more memory capacity on a single chip. Basic ground rules customarily imply more components for more capacity. Conventional unipolar or
bipolar memory cells employ either dynamic feedback stages whose stored information must be periodically refreshed (for synchronous operation) or with the use of multi-component flip-flop circuits (for asynchronous operation) which is more versatile.

Several independent physical phenomena in unipolar and bipolar semiconductor junction devices and integrated structures lead to voltage and current controlled negative resistance without the use of external feedback. These include avalanche breakdown, quantum mechanical tunneling, and minority carrier storage.

Two complementary generic types of negative resistance may be utilized as a basis for generating multistable energy levels. The number of stable states and their relative spacings can be readily varied. Additional stable states can be obtained with the use of negative resistance interactions and therefore the total amount of information that can be stored. This, in turn, facilitates a reduction in the number of active devices necessary to attain a given radix.

Such fundamental properties of negative resistances can be employed as a basis for multistable, e.g., ternary, quadristable and higher radix, solid state devices and integrated circuits.

A direct method to achieve further size reduction is to use a functional electronic memory device as the basic building block for the memory. Such a device provides the identical electronic memory function but necessitates only a small fraction of the number of components to do so and thereby offers the additional advantage of increased overall reliability.

The negative resistance devices discussed in this paper are such functional elements. Their memory capabilities permit operation asynchronously, whereby information may be stored or read out at will at rates from dc up to the device cut-off frequency.

Generally only a single negative resistance device is required per bit of memory as compared to a relatively large number of devices per bit for other forms of conventional semiconductor memory. This offers the intriguing possibility of a very dense array that occupies a small fraction of the chip area of conventional memories and with many times the random access capacity of standard semiconductor memory arrays presently available.

A parallel approach to increased memory capacity is through the use of higher order radices. Most present day digital computers are binary systems. This has been historically the case, since until devices or circuits capable of operation at radices higher than binary became available, the use of higher order radices for logic functions and for more efficient information storage had remained an academic matter.
The radix prescribes the quantity of digits employed in a given number system. To consider the relative storage efficiency of various radices, one may proceed as follows. Let I be the maximum amount of information that can be represented by n digits at radix R, where \( R^n = I \).

This is equivalent to the total number of different stable states of the digital devices comprising the system, assuming that the amount of equipment required to store information I is proportional to nR. In this case, two devices or units of equipment would be needed to store a bit, three for a ternary digit, etc.

To obtain a relative measure of storage efficiency we can hold I constant for variable radix R, so that \( \log I = n \log R \). Then the amount of equipment is proportional to \( \frac{R}{\log R} \). In order to determine the most efficient radix \( \log R \) should be minimized.\(^1\) The minimum occurs at \( R = e \) for which the nearest integral radix is three. Based, at least, on the assumption that the equipment varies as R, a radix of three would be more efficient from an equipment standpoint than a binary radix.

The use of ternary and higher order radices has generally been precluded in the past because of the non-availability of suitable devices or circuits. With the advent of new solid state negative resistance devices, however, the use of higher order radices for storage and other logic function now becomes feasible and offers intriguing advantages. The validity of the assumption that the equipment complexity is proportional to the product of n and R must be investigated for each configuration under consideration. For example, if n is the number of binary devices or circuits which can be integrated monolithically to form new devices which operate at radices higher than binary, then radices higher than ternary can become more efficient both from the standpoint of storage density as well as component-wise than either binary or ternary.

Let us consider, for example, the total information capability of a conventional integrated circuit binary 32-bit shift register. In this case \( R = 32 \) and \( n = 2 \). Hence, \( I = 2^{32} \approx 10^{10} \). If the radix were changed to six from binary, then \( I = 6^{32} \approx 10^{24} \). This indicates that by merely increasing the radix by four, an increase of fourteen orders of magnitude of information storage capability can be realized.

**Multistable States.** A direct way to generate multistable states is with the use of negative resistances. Multistable devices and circuits have two or more stable states of equilibrium for fixed supply voltage and circuit parameters. The states may be characterized by sets of stable voltages, currents, fluxes or oscillation frequencies.

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Bistability, the simplest form of multistability, has been used for many years in binary circuits, counters, storage components, and other elements of data systems.

To achieve multistability with negative resistance devices one must consider the more general problem of the interconnection of multiple devices which may or may not be turned to on or off states independently of whether the other negative resistance elements comprising the composite characteristic are on or off. In order to do so, it becomes apparent that the preferable configuration for multistable operation is (a) a connection for voltage controlled negative resistances, and (b) a parallel connection for current-controlled negative resistances.

The rationale for this is as follows. When one compares complementary negative resistances when operated bistably, the following basic differences become apparent. As the bias is increased from zero, the voltage-controlled negative resistance switches initially from a high conduction state to a high resistance state. The current-controlled negative resistance on the other hand switches from an initial high resistance state to a high conduction state as bias is increased.

If one considers a state of high conductance to be “on” and a state of high resistance to be “off”, then it becomes clear that the serial connection of voltage-controlled negative resistances or the parallel connection of current-controlled negative resistances can lead to multistability.

With idealized negative resistances the converse does not apply. For example, with the parallel connection of multiple voltage-controlled negative resistance devices, if one device were turned “on” to its high conduction state with the others remaining “off”, the latter would be shorted-out by the former.

Conversely, for the serial connection of multiple current-controlled devices normally in an “off” condition, an attempt to turn one negative resistance device “on” would be precluded by the “off” current limitation imposed the non-conducting devices.

The parallel connection of an array of devices is preferable to a serial connection from the standpoint of monolithic fabrication technology. Hence, current-controlled negative resistances (e.g., as exhibited in the avalanche transistor or the pnpn device) provides a basis for an integrated multistable array. Toward such an end, let us consider an array of pnpn devices on a common substrate as shown in Figure 1. These devices may be identical in which case associated passive integrated circuitry will be needed to provide a composite multistate characteristic. Alternately, such external circuitry can be minimized if the device’s negative resistance characteristics are appropriately graded across the array.
will be investigated initially. Shown in Figure 2 are two identical pnpn devices I and II integrated with common substrate regions P\(_2\) and N\(_2\). Diodes P\(_1\)N\(_1\) and P\(_3\)N\(_3\) are serially connected independently to the common substrate via junctions J\(_2\) and J\(_5\). The coupling between devices I and II is affected by a number of factors which have been analyzed as a basis for incorporating electrically built-in isolation or multistate operation. Shown in Figure 3 are two pnpn diodes in (a) and the equivalent circuit in part (b) of the figure. In a previous paper\(^2\) we considered the effect of avalanche multiplication on the device characteristic, as shown in equation 3.63 of Figure 4, where M\(_p\) and M\(_n\) are the voltage dependent multiplication factors for elections and holes. This equation is the general form of the device resistance, \(\frac{\delta V^2}{\delta I}\), in terms of the alphas and multiplication factors of a pnpn device. At reverse bias of the center junction, equation 3.63 reduces to 3.64, that \(\lambda_c = -1\) at negative biases. At the breakover point, \(\frac{\delta V^2}{\delta I} = 0\), and the numerator of equation 3.64 can be set equal to zero, as the denominator is now positive, and we obtain equation 3.65 as shown in Figure 4. In Figure 5 is shown the switching dynamics for a multistable voltage-controlled negative resistance characteristic and Figure 6 shows the tristable dynamics for the current-controlled case. Each negative resistance region is bounded by positive resistance regions as shown in Figures 5 and 6. In each case the number of positive resistance regions exceeds their negative resistance counterparts by one. Accordingly, it is apparent that the total number of stable states attainable with linear loads is M+1, where M is the number of negative resistance devices involved.

Analysis of the roots of characteristic equation of the multistable circuit as applied to the five regions, I-V, will determine the nature of the singularities at the points of intersection of the load line with the composite negative resistance characteristic. Several possible types of singularities must be investigated. For example, the solution will be a node if the roots are real and of identical sign. The node will be stable if the roots are negative, and unstable if positive. Real roots of opposite sign will result in a saddle point. Complex roots will define a vortex when pure imaginary, and a focus when complex conjugates. As was the case for nodes, foci will be stable when their real parts are negative and unstable when their real parts are positive. The slope of the root will be zero along the load line, namely, \(\frac{di}{de} = 0\), when \(R = -\frac{e}{r_1}\). Correspondingly, the slope of the root will be infinite along each negative resistance region, namely \(\frac{di}{de} = \infty\) when \(r_1 = e^i\). This applies to both negative resistance regions II and IV for which the load \(R_L\) \(\frac{R_{n_1}}{R_{n_2}}\). In each case, both roots are real and of opposite sign resulting in two saddles at points 2 and 4. In regions I, III, and V where the composite characteristic has resistances \(r_1\), \(r_3\) and \(r_5\) respectively, the roots are negative. Accordingly, in these regions stable nodes or foci will occur at points 1, 3, and 5. These are the points of system stability or stable states of the multistable circuit. In the case of the stable nodes the solutions are parallel to the \(m_1\) axes.

near the nodal points, namely for large values of time. Allowing a disturbance, Triggering of the multistable circuit may be effected by appropriate external stimuli, for example by a change in applied voltage. In triggering from a stable state in one region to another (see Figures 5 and 6) the time involved during transition is dependent upon the reactive elements of the circuit. The reactances also include internal device reactances and parasitics present externally.

To this point the multiple M+1 stable states generated due to the serial or parallel connection of appropriate multiple S- or N-type negative resistances were obtained with linear loads. Negative resistance interactions due to nega-resistance devices with interacting negative resistance loads will be considered in the next section.

**Negative Resistance Interactions.** In the graphical analysis of a device characteristic, the load is generally considered to be single valued if not linear at least in the vicinity of the operating point. In this section we shall consider the interaction of composite N and S type negative resistances with negative resistance loads. As was shown in the previous section the composite S or N characteristic may have N + 1 stable states where N is the number of negative resistance devices. With negative resistance interactions the additional number of stable states that result increases the radix and therefore the total amount of information that may be stored. This facilitates a reduction in the number of active devices necessary to attain a given radix.

**S-S Interaction.** Let us consider next the interaction of an S-type negative resistance with an S-type negative resistance load. Such an interaction is shown in Figure 7. The device characteristic in this case is represented by 0 - 1 - 6 - 5. The load at the first switching point 1 is given by negative resistance L - L. Switching occurs along this line, namely from 1 - 2 - 3 - 4, where the line segment 2 - 3 is an additional stable state. As the device characteristic is further traversed at higher negative voltages by the load, the operating point proceeds from 4 - 5, returning along this line to point 6 as the sweep voltage decreases. Switching occurs along line L’L’ namely from point 6 to 7 from which the operating point returns to the origin as the sweep voltage goes to zero.

Experimental examples of S-S interaction are shown in Figure 8 for multistable hole storage diodes connected in series.

**N-N Interaction.** In the Figure 9 an idealized N-type avalanche negative resistance is represented by the segments 0 - 1 - 6 - 5. Its load is also an N-type negative resistance along which switching occurs via segments 1 - 2 - 3 - 4. Segment 2 - 4 is stable and segments 1 - 2 and 3 - 4 are unstable. As the original N-type negative resistance is further traversed by the load, the operating point proceeds from 4 to 5. On the return sweep, it
goes to 6 via 4. At point 6 switching occurs to point 7. From this point on the operating point returns monotonically to the origin along 7 - 0 as the voltage is reduced to zero.

Experimental examples of N-N interactions for avalanche transistors are shown in Figures 10 and 11.

**S-N Interaction.** In the case of S-N interaction annihilation may occur. The sweep sequence is shown in Figure 12 before and after annihilation. Prior to annihilation the switching sequence is shown on the composite S-N characteristic in (a) of the figure. The sequence before annihilation is 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7 - 8 - 9 - 0. Following annihilation of the negative resistances, the sweep sequence becomes 0 - 1 - 5 - 6 - 0 over the remaining characteristic which is essentially linear.

If a voltage-controlled negative resistance characteristic is made to interact with that of a current-controlled negative resistance, annihilation of a portion of the composite characteristic may be possible. In order to accomplish this, the range or one or both of the negative resistance elements should be variable so to as to extend to the energy range of its counterpart. This may be readily accomplished if appropriate S and N-type negative resistances occur in the same device.

Let us consider a pnp transistor in which an N-type negative resistance occurs due to avalanche at the collector-base junctions. If the junction is also parametrically excited by a high frequency energy source or dynamic B+ to inject carriers at a rate high compared to the reciprocal of the effective lifetime of minority carriers in the high resistivity side of the junction, a voltage-controlled negative resistance will also appear in the composite characteristic. This is shown in Figure 13.

This method of negative resistance annihilation has been employed\(^3\) to provide a fast acting long life duplexer (high-low power switching device) for use at a variety of frequencies. Such a device changes from a high impedance to a low impedance upon the interaction and annihilation of the negative resistance characteristics exhibited in the composite characteristic.

**Increased Number of Stable States Due to Negative Resistance Interactions.** The maximum number of stable states with interactions that can be realized with M interacting negative resistance elements of a given type is as follows:

As was shown in the previous section the total number of non-interacting stable states is \(M + 1\). In addition, there will be \((M - 1)!\) interactions, if each negative resistance element is allowed to interact with each other one in its composite characteristic. This gives us a

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total number of possible states of:

\[ M + 1 + (M - 1)! = (M + 1) + \Gamma(M) \]

stable states where \( \Gamma \) represents a gamma function. Since

\[ M\Gamma(M) = \Gamma(M + 1) \]

to which is the maximum number of stable states that can be realized for an S - S or an N - N interaction.

Examples of multistable triggering are shown in Figures 14 and 15 where a two transistor avalanche circuit was employed to provide tristable counting shown in Figure 14. The (a) trace shows the untriggered ground state. Triggering to the first state is shown in trace (b) and to the second state in trace (c). Finally in the upper trace (d) is shown tristable counting which occurs cyclically in this case from 2 to 1 to 0.

A similar set of multistable counting wave forms from states 0 to 1 to 2 are shown in Figure 15 for a quadristable tunnel diode circuit of Figure 16. In traces (a) and (b) of the latter figure are shown the V-I characteristic of three tunnel diodes in serial connection. The (a) trace is magnified along the ordinate axis. Figure 16 (c) shows three astable frequencies that were obtained from the circuit as the voltage was swept through the three negative resistance regions of the composite characteristic. Each frequency could be tuned independently of those due to the other tunnel diodes comprising the composite V-I characteristic.

In Figure 17, subharmonic generation is shown with an avalanche trigger circuit. In Figure 17 (a), a bistable output is shown with no countdown. In (b) of the figure is represented a countdown ratio of 1:2 for a pulse-to-trigger ratio of 1:4. Finally, in (c) of the figure the oscilloscope photograph of a 1:3 countdown ratio is shown. The following Figure 18 shows an additional feature of the multistable circuit, namely the combination of subharmonic generation and astable oscillation, for no countdown in (a) of the figure and for 1:2 countdown in (b).

**Integrated Devices.** Three-quarter inch diameter commercially-obtained silicon wafers were used in this investigation to fabricate multiple avalanche negative resistance elements on a common substrate. Three epitaxial layers were grown on <100> silicon to provide a
total of four regions (pnpn) following which the top and bottom surfaces were plated (by evaporation) with a gold film to give an overall thickness of approximately .002 mils.

Silicon pn-pn slices with 20-volt breakover characteristics were employed for monolithic fabrication of up to 200 individual devices on a common substrate. Resulting devices were made in various areas from 2 mils square to 8 mils square and in various configurations and spacings. Each new device had essentially the same breakover voltage as its large area counterpart. The composite structures were mounted in a 14 lead flat package (see upper photograph of Figure 19). To do so, the common cathode structure was bonded to the insulating header substrate, the common cathode, and the anodes were individually thermocompression bonded to the header pins with 2 mil gold wire.

Experimental arrays of pn-pn diodes which were fabricated by a combination of diffusion and epitaxial growth techniques with an H-geometry on a common substrate as shown in the lower photograph of Figure 19 were also operated multistably.

For the fabrication of integrated tunnel diodes on a common substrate, a 10 mil thick slice of \(<100\>\) germanium doped with \(10^{19}\) donors per cc. and with a resistivity of .0007 ohm centimeter was scribed into 20 mil square dice. The anodes were made of indium pellets of from 0.5 to 3 mils in diameter. The pellets were alloyed into the germanium substrate by quadruple focused infrared sources under vacuum of approximately 50 microns at a temperature of 300°C for approximately 10 seconds. The process produced multiple tunnel diodes with an average peak current and peak to valley ratio of 7 to 1.

From the large yield of diodes on the germanium substrate, seven were selected with similar characteristics. The base material was connected to the header which served as a cathode. Anode connections were made by thermocompression bonding with 2 mil gold wire to the alloyed indium pellets which served as anodes (see Figure 20). Although diodes of similar characteristics were selected, it was necessary to employ a variable resistor across each diode to compensate for individual variations in their characteristics.

**Conclusion.** Radices higher than binary are now achievable with present-day technology. For example, multistable circuits can readily be built from unipolar and bipolar semiconductor negative resistance building blocks. The complementary features of voltage-controlled and current-controlled negative resistance devices allow versatility in the design of multistate circuits. Examples include the serial connection of voltage-controlled or the parallel connection of current-controlled negative resistances which can result in composite characteristics with one more state than the number of negative resistances involved. With S-S or N-N negative resistance interactions additional states occur, whereas with an S-N interaction, annihilation of the S and N negative resistance regions is effected. Further reduction in circuit complexity results directly from tristable
and quadrastable operation with single devices. By device design or electrical modification of device characteristics the value of negative resistance and the spacings between stable states can be varied to accommodate triggering, provide desired output voltage levels, or result in operation in several digital and analog modes. The semiconductor junction devices employed lend themselves effectively to monolithic array integration utilizing integrated circuit technology. The isolation that is provided electrically offers the advantage over conventional isolation techniques that no additional processing steps are required.

There is still further work to be done in the area of the research. For example, as the radix increases the constraints on the effects of noise, composite device triggering, load linearity, and power supply regulation requirements become more stringent and therefore impose more critical integrated circuit design requirements. There is also a parallel need for the further development of higher order logic as an extension of Boolean logic. This is needed to describe the operation of specific multistate devices and circuits in order to increase their compatibility with existing binary systems.

The utilization of multistable devices and integrated circuits treated in this paper offers a number of intriguing advantages. With such technology it is possible to achieve appreciable circuit simplicity, higher storage density, increased reliability, and reduced cost over conventional circuitry for many useful applications. The multistable building blocks used to accomplish this, serve as the basis for multifrequency oscillators, variable gain amplifiers, variable radix-frequency multipliers and dividers, dense memory storage, and other analog and digital functions with radices higher than binary.

Figure 1
Monolithic Avalanche Array
Figure 2
Multistable Avalanche Circuit
(a) Integrated Dual Avalanche pn-pn Diode

(b) Equivalent Circuit
Integrated Dual PNPN Diodes and Equivalent Circuit

Figure 3
PWN Avalanche Device

\[ I = a_N I_N + a_P I_P - I_{co} \lambda_2 \]  
(3.38)

With avalanche multiplication

\[ \frac{\partial V_2}{\partial I} = \frac{1 - M_N \left( a_N + I \frac{\partial a_N}{\partial I} \right) - M_P \left( a_P + I \frac{\partial a_P}{\partial I} \right)}{I \left( M_N \frac{\partial a_N}{\partial V_2} + M_P \frac{\partial a_P}{\partial V_2} + a_N \frac{\partial I}{\partial V_2} + a_P \frac{\partial I}{\partial V_2} \right) - \frac{\partial I}{\partial V_2} \frac{e_{co} \lambda_C}{I_{co}} - \frac{\partial \lambda_C}{\partial V_2} } \]  
(3.63)

At reverse bias of the center junction

\[ \frac{\partial V_2}{\partial I} = \frac{1 - M_N \left( a_N + I \frac{\partial a_N}{\partial I} \right) - M_P \left( a_P + I \frac{\partial a_P}{\partial I} \right)}{I \left( M_N \frac{\partial a_N}{\partial V_2} + M_P \frac{\partial a_P}{\partial V_2} + a_N \frac{\partial I}{\partial V_2} + a_P \frac{\partial I}{\partial V_2} \right) - \frac{2 \partial V_2}{\partial I}} \]  
(3.64)

At the breakover point \( \frac{\partial V_2}{\partial I} = 0 \) and the numerator of equation (3.64) can be set equal to zero as the denominator is now positive. Hence

\[ 1 - M_N \left( a_N + I \frac{\partial a_N}{\partial I} \right) - M_P \left( a_P + I \frac{\partial a_P}{\partial I} \right) = 0. \]  
(3.65)

FIGURE 4

TRISTABLE TRANSIENT DYNAMICS
VOLTAGE-CONTROLLED NEGATIVE RESISTANCE WITH THREE STABLE NODES AND TWO SADDLE POINTS.

FIGURE 5
TRISTABLE TRANSIENT DYNAMICS
CURRENT-CONTROLLED NEGATIVE RESISTANCE WITH
THREE STABLE NODES AND TWO SADDLE POINTS.

FIGURE 6

S-S NEGATIVE RESISTANCE INTERACTION AND
SWITCHING SEQUENCE

FIGURE 7
(d) Four Stable States
Due to Negative Resistance Interaction
DB+ = 2v @ 150mc

(c) Tristable Characteristic
DB+ = 2v @ 150mc

(b) Two Negative Resistances at Different Energy Ranges
DB+ = 2v @ 150mc

(a) Static Characteristic
DB+ = 0

INTERACTION OF TWO VOLTAGE CONTROLLED NEGATIVE RESISTANCES
FIGURE 8

N-N NEGATIVE RESISTANCE INTERACTION AND SWITCHING SEQUENCE
FIGURE 9
N-N NEGATIVE RESISTANCE INTERACTIONS DUE TO PARALLEL CONNECTIONS OF TWO AVALANCHE TRANSISTORS

FIGURE 10

Vertical Scale: 5 v/cm; Horizontal Scale: 0.5 ma/cm
R_2: Varied; R_3 and R_4 = 50 Ohms; R_s = 500 ohms.
N-N NEGATIVE RESISTANCE INTERACTIONS DUE TO PARALLEL CONNECTION OF FIVE AVALANCHE TRANSISTORS

FIGURE 11
S-N INTERACTIONS IN AVALANCHE TRANSISTOR

**FIGURE 13**

- (a) Negative Resistance Annihilation
  - 20 ma/cm

- (b) Partial Interaction

- (c) Negative Resistance Switching (non-interacting)
  - 7 V/cm
  - Rs = 10K
  - DB+freq. = 10mc

- (d) S & N Negative Resistance in Single Device Characteristic
TRIGGERING OF TRISTABLE AVALANCHE MULTIVIBRATOR

FIGURE 14

(d) Tristable Counting

(c) Triggering to Second State

(b) Triggering to First State

(a) No Trigger (Ground State)

Vertical Scale: 1 v/cm
Horizontal Scale: 600 μsec/cm
Trigger: 1/2 μ sec @ -2v
@ 1246 cps
TUNNEL DIODE TRISTABLE TRIGGERING

FIGURE 15
TUNNEL DIODE MULTIFREQUENCY OSCILLATOR

FIGURE 16
AVALANCHE SUBHARMONIC GENERATION

FIGURE 17

(a) No Countdown
   (1:2 Pulse to
   Trigger Ratio)

(b) 1:2 Countdown
   (1:4 Pulse to
   Trigger Ratio)

(c) 1:3 Countdown
   (1:6 Pulse to
   Trigger Ratio)

Vertical Scale: 1 v/cm
Horizontal Scale: 600 μsec/cm
Pulse Repetition Rate: 1250 cps
(a) Astable Triggering
   No countdown

(b) Astable Triggering
   1 : 2 Countdown

Vertical Scale: 1v/cm
Horizontal Scale: 600 usec/cm
Repetition Rate: 1250 cps
Astable Oscillation Frequency: 120kc

AVALANCHE ASTABLE SUBHARMONIC GENERATION
FIGURE 18
FIGURE 19
MONOLITHIC TUNNEL DIODE ARRAYS
FIGURE 20